ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Decoupling the Bias-Stress-Induced Charge Trapping in Semiconductors and Gate-Dielectrics of Organic Transistors Using a Double Stretched-Exponential Formula

Hyun Ho Choi, Moon Sung Kang, Min Kim, Haena Kim, Jeong Ho Cho, and Kilwon Cho**

A novel strategy for analyzing bias-stress effects in organic field-effect transistors (OFETs) based on a four-parameter double stretched-exponential formula is reported. The formula is obtained by modifying a traditional single stretched-exponential expression comprising two parameters (a characteristic time and a stretched-exponential factor) that describe the bias-stress effects. The expression yields two characteristic times and two stretched-exponential factors, thereby separating out the contributions due to charge trapping events in the semiconductor layer-side of the interface and the gate-dielectric layer-side of the interface. The validity of this method was tested by designing two model systems in which the physical properties of the semiconductor layer and the gate-dielectric layer were varied systematically. It was found that the gate-dielectric layer, in general, plays a more critical role than the semiconductor layer in the bias-stress effects, possibly due to the wider distribution of the activation energy for charge trapping. Furthermore, the presence of a self-assembled monolayer further widens the distribution of the activation energy for charge trapping in gate-dielectric layer-side of the interface and causes the channel current to decay rapidly in the early stages. The novel analysis method presented here enhances our understanding of charge trapping and provides rational guidelines for developing efficient OFETs with high performance.

1. Introduction

Organic field-effect transistors (OFETs) have attracted attention in recent decades for their utility in flexible large-area displays, radio-frequency identification (RF-ID) tags, and sensors.[1–4] OFET fabrication processes are easily adapted to low-cost solution processes and printing techniques; however, the field-effect mobility (the key device parameter in FETs) of classical OFETs has remained low compared to their inorganic counterparts, i.e., amorphous silicon-based transistors (with field-effect mobilities of 1–10 $cm^2\ V^{-1}\ s^{-1}$), preventing their commercialization. A variety of research have been conducted in an effort to improve the performance of OFETs.[5–7] To this end, new semiconducting organic materials have been synthesized,[8–10] methods have been developed for controlling the electrode/semiconductor and semiconductor/gate-dielectric interfaces,[11–14] charge transport physics have been studied,[15–17] and new device architectures have been designed.[18–20] As a result of these efforts, OFETs with high field-effect mobilities above 1 $cm^2\ V^{-1}\ s^{-1}$ are now achievable using conjugated small molecules and polymers.

In addition to the field-effect mobility, improving device stability is of another crucial importance for achieving practical applications of OFETs. In particular, a drop in the channel current and a detrimental shift in the threshold voltage, named as the bias-stress effect, are typically observed in OFETs operating under a continuous applied bias.[21,22] Such degradation in the device performances is thought to originate from charge trapping in the devices.[23–25] To date, however, a clear understanding of the physical mechanisms underlying charge trapping is still lacking. Considering that charge transport and trapping in an OFET take place at the semcionductor/gate-dielectric interface,[26,27] which is formed from a physical contact of two layers, decoupling the role of the two materials in interfacial charge trapping is crucial. However, their relative contributions have not been fully understood primarily due to the absence of a simple and appropriate analysis method.

H. H. Choi, M. Kim, H. Kim, Prof. K. Cho
Department of Chemical Engineering
Center for Advanced Soft Electronics (CASE)
Pohang University of Science
and Technology (POSTECH)
Pohang 790-784, Korea
E-mail: kwcho@postech.ac.kr
Prof. M. S. Kang
Department of Chemical Engineering
Soongsil University
Seoul 156-743, Korea
Prof. J. H. Cho
SKKU Advanced Institute of Nanotechnology (SAINT)
and Center for Human Interface Nano Technology (HINT)
School of Chemical Engineering
Sungkyunkwan University
Suwon 440-476, Korea
E-mail: jhcho94@skku.edu

DOI: 10.1002/adfm.201201545

Here, we present a novel strategy for analyzing the bias-stress effects in OFETs based on a four-parameter double stretched-exponential formula. The formula was obtained by modifying a traditional single stretched exponential expression with two parameters (a characteristic time and a stretched-exponential factor), which was then used to describe the bias-stress effects. The expression separated the contributions of the charge trapping events at the semiconductor layer-side of the interface and the gate-dielectric layer-side of the interface (requires two characteristic times and two stretched-exponential factors). The properties of two separate OFETs that shared a common semiconductor layer but were independently gated by a conventional SiO_2 gate-dielectric and a vacuum gap gate-dielectric were experimentally investigated and analyzed. Because the gate-dielectric layer in the vacuum gap-gated OFETs cannot physically contain any carrier traps, this device was used to determine the two parameters corresponding to charge trapping effects resulting exclusively from the semiconductor layer-side of the interface. These values, along with the analysis results from conventional SiO_2-gated OFETs, permitted calculation of the other two parameters corresponding to the charge trapping in the gate-dielectric layer-side of the interface. To ensure the validity of this method, we designed two model systems in which the physical properties of the semiconductor layer and the gate-dielectric layer were varied systematically. The double stretched-exponential fitting parameters extracted from these systems varied in accordance with the expected trends. This novel method permits a deeper understanding of the bias-stress effects in OFETs and thus, can potentially contribute to enhancing the device performance.

2. Results and Discussion

Typically, the bias stress-induced drain current (I_D) decay in OFETs is described by a stretched-exponential time (t)-dependent formula applicable to a wide variety of disordered systems:[21,28,29]

$$I_D(t) = I_D(0)\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \quad (1)$$

where $I_D(0)$ is the initial drain current at $t = 0$, β is the dispersion parameter of the barrier energy height for charge trapping, and τ is a characteristic time associated with the rate of charge trapping. The time-dependence of this is determined from the changes observed in the free carrier density (N_f) upon application of gate bias through charge trapping, expressed as[21,28,30]

$$d\Delta N_f/dt = -AD\Delta N_f \quad (2)$$

where A is a proportionality constant and D is the time-dependent diffusivity ($D = D(t)$) which represents the rate of free carrier diffusion into the traps.[31] Although this expression was originally developed to describe the bias-stress effect in amorphous silicon transistors considering the time-dependent evolution of trap states due to hydrogen migration,[28] we can employ similar mathematical formula to describe dispersive trapping process in OFETs. A detailed derivation of Equation (1) is provided in the Supporting Information. Despite the utility of this formula, it should be noted that an analysis based on Equation (1) cannot decouple the contributions due to charge traps located in the semiconductor layer-side of the interface versus those in the gate-dielectric layer-side of the interface, both of which are critical for OFET operation. This model cannot decouple the effects because the method employs only a single parameter D and, thus, a single set of β and τ parameters describes the net carrier diffusion properties regardless of the trap locations.

For more careful analysis to understand the charge trapping mechanism and the resulting bias-stress effect in an OFET, it is required to separate the semiconductor layer and the gate-dielectric layer contributions for charge trapping. We modified the traditional model described above to distinguish the charge trap sites located in the semiconductor layer-side and those in the gate-dielectric layer-side. Separate diffusivities of the free carriers in each medium (semiconductor or gate-dielectric) were considered: D_S and D_{GD} represent the diffusion of the free carriers within the semiconductor and the gate-dielectric layers, respectively. As a first-order approximation, we assumed that the effective diffusivity (D^*) of the free carriers at the semiconductor/gate-dielectric interface is a linear combination of D_S and D_{GD} ($D^* = aD_S + bD_{GD}$, where a and b are the weighing factors of each contribution). Using this expression, Equation (2) can be modified as

$$d\Delta N_f/dt = -A[a\,D_S(t) + b\,D_{GD}(t)]\,\Delta N_f \quad (3)$$

Moreover, the transient current behavior can then be described by a double stretched-exponential formula, given as

$$I_D(t) = I_D(0)\exp\left[-\left(\frac{t}{\tau_S}\right)^{\beta_S}\right]\exp\left[-\left(\frac{t}{\tau_{GD}}\right)^{\beta_{GD}}\right] \quad (4)$$

where β_S and β_{GD} represent the dispersion parameters describing the distribution of activation energy for charge trapping in the semiconductor layer-side of the interface and the gate-dielectric layer-side of the interface, respectively and τ_S and τ_{GD} represent the characteristic time constants for charge trapping events that occur at charge traps in the semiconductor layer-side of the interface and the gate-dielectric layer-side of the interface, respectively. The derivation of Equation (4) from Equation (3) is provided in the Supporting Information.

Experimentally, one could, of course, obtain four fitting parameters (β_S, β_{GD}, τ_S, and τ_{GD}) from a single bias-stress experiment on a conventional OFET. Despite the simplicity of this approach, the physical interpretation of the parameters can be ambiguous as the number of fitting parameters increases. Instead, we prepared two different types of OFETs for a given semiconductor material in an effort to obtain more reliable fitting parameters: one device was based on a conventional gate-dielectric, e.g., a SiO_2 layer, and the other was based on a vacuum gap gate-dielectric. The merits of testing a vacuum gap-gated OFET are that such device structures cannot physically possess charge traps in the gate-dielectric layer (because it is a vacuum).[32–34] Therefore, the second exponential decay term on the right hand side of Equation (4) becomes unity. The transient behavior of a vacuum gap-gated OFET can then be described by

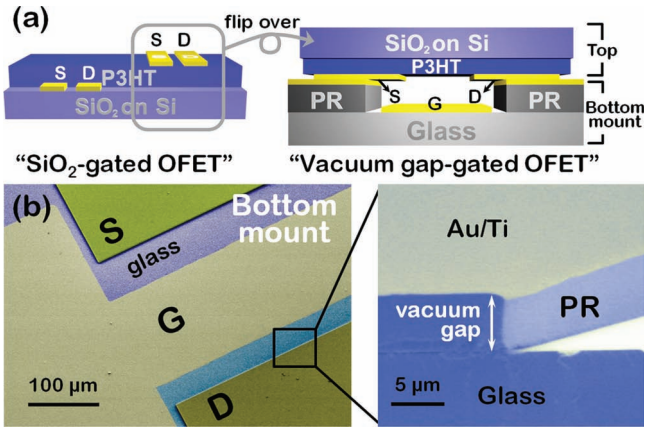

Figure 1. a) Schematic diagram of the bottom-contact P3HT OFETs fabricated with SiO_2 and vacuum gap gate-dielectrics. b) Scanning electron microscopy images of the vacuum gate-dielectric mount.

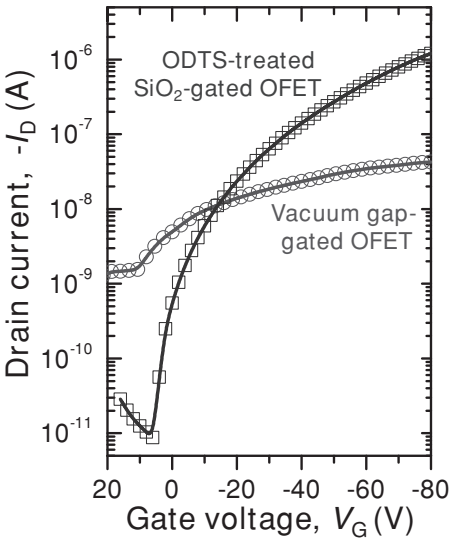

Figure 2. Transfer characteristics of the OFETs, based on a P3HT film with an ODTS-treated SiO_2 gate-dielectric (rectangles, at $V_D = -80$ V) and a vacuum gap gate-dielectric (circles, at $V_D = -40$ V).

$$I_D(t) = I_D(0)\exp\left[-\left(\frac{t}{\tau_S}\right)^{\beta_S}\right] \quad (5)$$

which allows the extraction of the two fitting parameters (β_S and τ_S) associated solely with the nature of charge traps in semiconductor layer-side of the interface. Once these parameters are obtained, the other two parameters associated with charge traps in gate-dielectric layer-side of the interface (β_{GD} and τ_{GD}) could be readily obtained by measuring the I_D decay in a conventional OFET. Once the parameters (β_S and τ) are known, the fitting problem then becomes a two-parameter problem that should yield more reliable fitting results than would be expected from a four-parameter fitting problem.

A schematic diagram of the OFETs based on a poly(3-hexylthiophene) (P3HT) semiconductor is displayed in **Figure 1**a. Conventional oxide-gated OFETs were prepared on a highly doped *n*-type Si wafer (that served as the gate electrode for the SiO_2 gating) with a thermally grown 300-nm-thick SiO_2 layer (gate-dielectric). The measured capacitance of the SiO_2 gate-dielectric was 10.8 ± 0.2 nF cm^{-2} (Figure S1, Supporting Information). The influence of the SiO_2 surfaces on the charge trapping properties was tested by treating some of the wafers with octadecyltrichlorosilane (ODTS) according to a method described previously.[35–38] Onto the wafers with or without the ODTS layer, bottom-contact Au/Ti source/drain electrodes were deposited via thermal evaporation through a shadow mask. A P3HT layer was then spin-coated to form a conventional bottom-contact bottom-gate OFET.

A vacuum gap-gated OFET based on the as-spun P3HT layer was prepared by depositing a second set of Au source/drain electrodes onto the P3HT layer. The distance between the SiO_2-gated channel and the vacuum gap-gated channel on the common P3HT layer was small (<1 mm), considering that the subsequent bias-stress experiments were carried out on the same P3HT layer. Separately, a vacuum gap gate-dielectric mount, equipped with a trough (depth = 5.1 μm) that later served as the vacuum gap gate-dielectric and patches for the source/drain and gate contacts were prepared on a glass substrate using photolithography (see the scanning electron microscopy (SEM) image of the vacuum gap gate-dielectric mount in Figure 1b). The measured capacitance of the vacuum gap gate-dielectric at 1 MHz was 0.19 ± 0.04 nF cm^{-2} (Figure S1, Supporting Information). The as-prepared substrates with the P3HT layers and the Au electrodes were then flipped over and placed on the vacuum gap gate-dielectric mount to yield a vacuum gap-gated OFET based on the same P3HT film that was used to prepare the SiO_2-gated device.

The drain current (I_D) vs gate voltage (V_G) plots, measured at a constant drain voltage (V_D), for the ODTS-treated SiO_2-gated and vacuum gap-gated OFETs with as-spun P3HT films are shown in **Figure 2**. The ODTS-treated SiO_2-gated OFET produced a typical I_D–V_G curve with good current modulation (rectangular data points) and a field-effect mobility up to 3.0 × 10^{-3} cm^2 V^{-1} s^{-1}.[39–40] By contrast, the vacuum gap-gated OFET yielded much weaker current modulation (circular data points). Such a weak current modulation is consistent with previous results based on vacuum gap gate-dielectrics, possibly due to the low capacitance of the gate-dielectric.[33]

The bias-stress effects of the P3HT OFETs were investigated by monitoring the I_D decay under a constant applied gate bias. **Figure 3** shows the normalized I_D decay in the P3HT OFET prepared on an ODTS-treated SiO_2 gate-dielectric under sustained gate and drain voltages of –80 and –10 V, over a period of 20 min (the raw data before normalization is shown in Figure S2, Supporting Information). The measurements were performed under vacuum (10^{-6} Torr) to exclude the influence of semiconductor degradation in air.[41–42] The curves A and B in Figure 3 show the normalized drain current decay of the vacuum gap-gated OFET and the ODTS-treated SiO_2-gated OFET, respectively. The latter decayed more than the former, indicating that a higher number of charge trapping events occurred in the ODTS-treated SiO_2-gated OFET than in the vacuum gap-gated OFET.

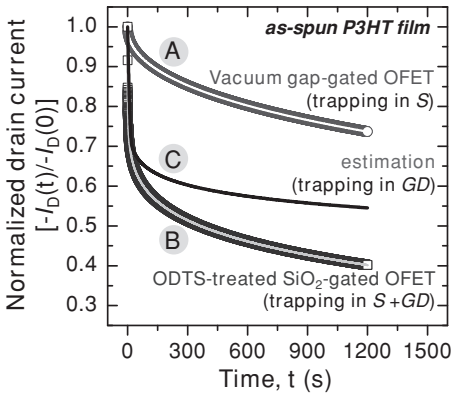

Figure 3. Normalized current ($-I_D(t)/-I_D(0)$) decay for the vacuum gap-gated OFET (curve A) and the ODTS-treated SiO_2-gated OFET (curve B). The current decay of curve A with the circular data points is associated with charge trapping in the semiconductor layer-side (S) of the interface, whereas the current decay of curve B with rectangular data point arises from charge trapping in both the semiconductor layer-side of the interface and the gate-dielectric layer-side (GD) of the interface. Curve C, which represents the current decay due to the charge traps located in the gate-dielectric layer-side of the interface, is produced from an estimate based on the double stretched-exponential formula described in the text.

As discussed above, the I_D decay of the vacuum gap-gated OFET (curve A in Figure 3) could be described by Equation (5), which yielded β_S and τ_S values of 0.47 and 1.5×10^4 s, respectively. These values, in combination with Equation (4), yielded a two-parameter fit to the I_D decay in a conventional ODTS-treated SiO_2-gated OFET (curve B in Figure 3). This yielded β_{GD} and τ_{GD} of 0.13 and 5.5×10^4 s, respectively. These values are summarized in **Table 1**. The β_{GD} and τ_{GD} values were used to determine the bias-stress effects due to the charge traps located in the gate-dielectric layer-side of the interface (the ODTS-treated SiO_2 layer) via the stretched-exponential with parameters associated solely with the gate-dielectric layer: $\exp[-(t/\tau_{GD})^{\beta_{GD}}]$ (curve C in Figure 3). From the fact that the magnitude of curve C was lower than that of curve A (at least during the initial 20 min), the charge traps located in the gate-dielectric layer-side of the interface (the ODTS-treated SiO_2 layer) were found to contribute more significantly to the current decay than those in the semiconductor layer-side of the interface (the P3HT layer) in a P3HT OFET on the time scale of the experiment. These results were consistent with previous reports based on scanning Kelvin probe microscopy analysis, which concluded that the carrier trapping was more influenced by the gate-dielectric layer than by the morphology of the semiconductor.[24,43]

Table 1. Summary of the characteristic times (τ) and the dispersion parameters (β) for the semiconductor and the gate-dielectric layers in three different P3HT OFETs.

Film Type	Semiconductor Layer		Gate-Dielectric Layer	
	τ_S [$\times 10^4$ s]	β_S	τ_{GD} [$\times 10^4$ s]	β_{GD}
P3HT on ODTS-treated SiO_2	1.5	0.47	5.5	0.13
Annealed P3HT on ODTS-treated SiO_2	7.8	0.49	5.3	0.12
P3HT on bare SiO_2	1.6	0.52	0.5	0.48

The shapes of the curves indicated that the rapid I_D decay in the ODTS-treated SiO_2-gated P3HT OFET (curve B in Figure 3) in the early stages ($t < 100$ s) is most likely originated from charge trapping in the gate-dielectric layer-side of the interface (the ODTS-treated SiO_2 layer). An abrupt I_D decay was observed in curve C but not in curve A, as shown in Figure 3. The initial decay in a stretched-exponential formula is strongly coupled to the β value, such that smaller β value yields more rapid decays, particularly during the early stages of a current decay. Because β represents the distribution of the activation energy for charge trapping (ΔE_B), following the relation, $\Delta E_B = k_B T/\beta$, where k_B is the Boltzmann constant, our results indicate a wider distribution for the activation energy for charge trapping in the ODTS-treated SiO_2 layer ($k_B T/\beta_{GD} = 0.20$ eV) than in the P3HT layer ($k_B T/\beta_S = 0.05$ eV). Previous studies showed that the mean activation energy for charge trapping (E_B) in the OFETs are in the range of 0.4–0.8 eV,[21,29] much higher than the thermal kinetic energy of the charge carriers (0.02–0.03 eV). Thus, in general, charge carriers cannot instantly overcome the activation energy for charge trapping; however, an ODTS-treated SiO_2 layer that has a sufficiently wide distribution of the activation energy for charge trapping includes a low-energy barrier tail that is comparable to the thermal kinetic energy of the charge carriers. Rapid charge trapping in ODTS-treated SiO_2 gate-dielectrics is then allowed in the early stage of bias stress.

We further examined the gate voltage-dependence and thereby investigated the carrier concentration-dependence of the transient current behavior for both the vacuum gap-gated and ODTS-treated SiO_2-gated OFETs. Figure S3a,b (Supporting Information) display the transient drain current decay for the P3HT OFETs gated with vacuum gap and ODTS-treated SiO_2, respectively, at varying gate voltages. No obvious influence of the gate voltage on the bias-stress effect was observed, consistent with previous reports.[21,29,30,44,45] Accordingly, β and τ values for semiconductor and gate dielectric layers extracted from the method described above based on a double stretched-exponential formula exhibit no significant variation upon varying gate voltage (and thus carrier concentration) (Figure S3c, Supporting Information). Consequently, the results showing little influence of carrier concentration on transient current behavior support validity of utilizing β and τ values from the vacuum gap-gated device to estimate β and τ values for ODTS-treated SiO_2-gated device.

To further confirm the validity of the double stretched-exponential formula, two additional sets of experiments were carefully designed. The experiment and analysis described above were first applied to P3HT OFETs (**Figure 4**a,b), in which the semiconductor layer was thermally annealed (at 170 °C for 15 min). The thermal annealing enhanced the crystallinity of the P3HT layer, as confirmed by atomic force microscopy images and X-ray analysis, shown in Figure S4 (Supporting Information). Despite the enhanced semiconductor crystallinity, however, thermal annealing of the semiconductor layer was not expected to influence the nature of charge trapping events that occurred at the gate-dielectric layer-side of the interface. The values of β_{GD} and τ_{GD} that described the I_D decay were expected to remain unchanged upon thermal annealing. By contrast, the values of β_S and τ_S were expected to change noticeably after annealing.

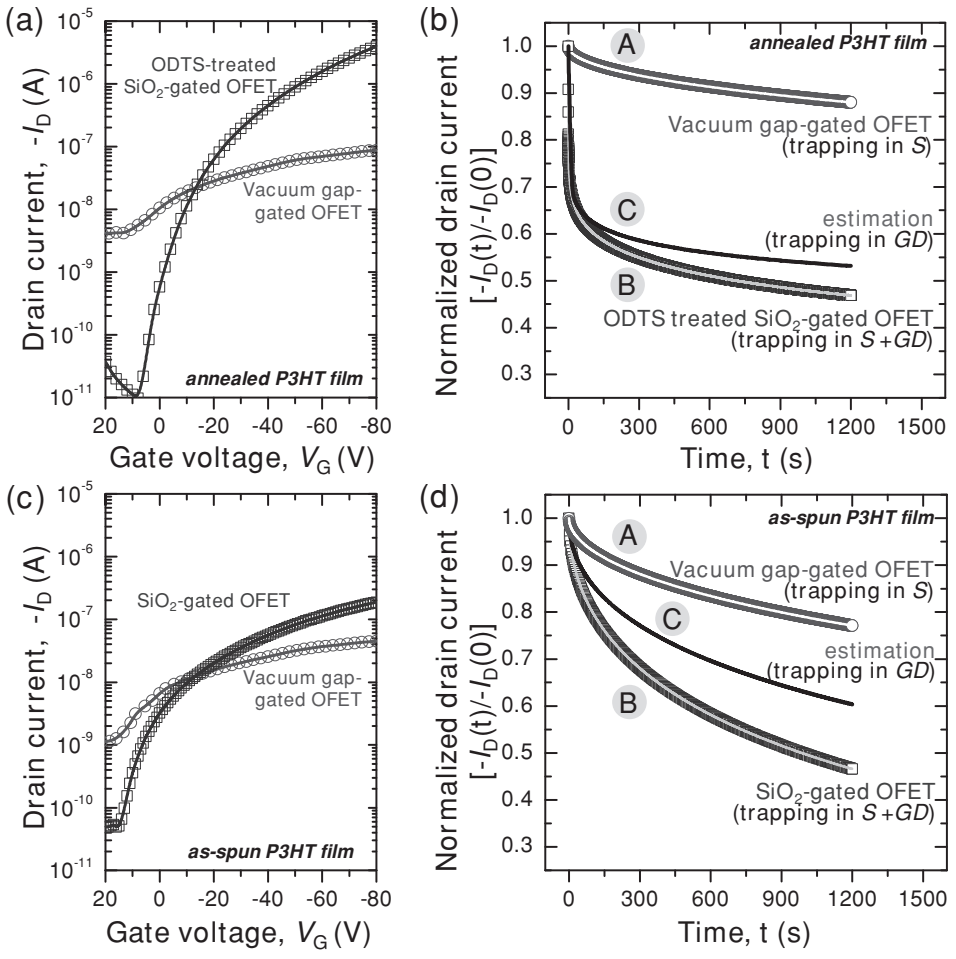

Figure 4. a) Transfer characteristics of thermally annealed P3HT OFETs gated with ODTS-treated SiO_2 (rectangles, at $V_D = -80$ V) or vacuum gap (circles, at $V_D = -40$ V) gate-dielectric. b) Normalized current ($-I_D(t)/-I_D(0)$) decay for OFETs in (a) gated with vacuum gap (curve A) or ODTS-treated SiO_2 (curveB) gate-dielectric. c) Transfer characteristics of the as-spun P3HT OFETs gated with a bare SiO_2 (rectangles, at $V_D = -80$ V) or a vacuum gap (circles, at $V_D = -40$ V) gate-dielectric. d) Normalized current ($-I_D(t)/-I_D(0)$) decay for OFETs in (c) gated with vacuum gap (curve A) or bare SiO_2 (curveB) gate-dielectrics. In (b,d), curves C indicate the estimated current decay due to the charge traps located in the gate-dielectric layer-side of the interface.

The experiments on annealed P3HT OFETs yielded fitting parameters that were consistent with our expectations. First, significant variations in τ_S were obtained (7.7×10^4 s from an annealed P3HT OFET compared with 1.4×10^4 s from the as-spun P3HT OFET). These results indicate that the activation energy for charge trapping in the semiconductor layer-side of the interface is greatly enhanced or the density of charge trap sites is reduced upon thermal annealing, probably due to the improved crystallinity of the P3HT layer. Second, we observed that the values of β_S did not change significantly upon P3HT annealing (0.49 from the annealed P3HT OFET compared with 0.47 from the as-spun P3HT OFET). Such a subtle change in the β_S values suggest that the distribution of the activation energy for charge trapping in the P3HT layer did not vary significantly even are thermal annealing. Lastly and most interestingly, the values of β_{GD} and τ_{GD} were nearly constant before and after thermal annealing (β_{GD} and τ_{GD} of 0.12 and 5.3×10^4 s, respectively, from an annealed P3HT OFET compared with 0.13 and 5.5×10^4 s, respectively, from a pristine P3HT OFET). Taken together, these results support the use of a double stretched-exponential formula to describe charge trapping in OFETs.

Second, we applied the double stretched-exponential analysis to bias-stress experiments based on as-spun P3HT OFETs without an ODTS layer (Figure 4c,d). This set of experiments can be thought of as varying the nature of the gate-dielectric layer while retaining the properties of the semiconductor layer. If the double stretched-exponential formula were valid, of course, one would expect noticeable variations in the values β_{GD} and τ_{GD} but not β_S and τ_S. The as-spun P3HT OFETs without ODTS interlayer yielded β_{GD} and τ_{GD} values of 0.48 and 5.0×10^3 s, respectively, and β_S and τ_S of 0.52 and 1.6×10^4 s, respectively. As expected, the β_S and τ_S values did not vary significantly with the surface properties of the SiO_2 layer (compare the curves A in Figure 3 and Figure 4d), whereas the values of β_{GD} and τ_{GD} were significantly different (compare the curves C in Figure 3 and Figure 4d), again confirming the validity of the double stretched-exponential formula. Because β_{GD} decreased

from 0.48 to 0.13 and τ_{GD} increased from 5.0×10^3 to 5.5×10^4 s upon inserting the ODTS interlayer, we concluded that introducing the ODTS layer widened the distribution of the activation energy for charge trapping in the gate-dielectric layer-side of the interface and resulted in a more rapid I_D decay, particularly during the early stage of the bias stress. Furthermore, ODTS-treated SiO_2 has been revealed to have lower activation energy for charge trapping than bare SiO_2.[44] Therefore, the ODTS-treated SiO_2 requires less time for charge trapping. However, once charge carriers are trapped, the trapped charges in ODTS-treated SiO_2 layer-side of the interface were revealed to be more rapidly released than those in bare SiO_2 due to lower energy barrier for detrapping.[46] Hence, compared to the net charges trapped in bare SiO_2 layer-side of the interface, those trapped in ODTS-treated SiO_2 layer-side of the interface would increase slower with bias stress time except during the early stages. Consistently, the curves in Figure 3 and Figure 4d imply that the ODTS-treated SiO_2-gated OFETs would be more stable at the long time scale ($t > 2000$ s) than the bare SiO_2-gated OFETs.

3. Conclusions

We developed a novel method for investigating the bias-stress effects in OFETs by employing a double stretched-exponential formula. This method permitted us to separately describe charge trapping in the semiconductor layer-side of the interface and the gate-dielectric layer-side of the interface in OFETs. The systematic results obtained from examination of P3HT OFETs prepared in three different methods including an ODTS-treated SiO_2 gate-dielectric/vacuum gap gate-dielectric, an as-spun P3HT/annealed P3HT, and an ODTS-treated SiO_2/bare SiO_2, confirmed the validity of the method. The gate-dielectric layer-side of the interface, in general, plays a more critical role than the semiconductor layer-side of the interface in the bias-stress effects, possibly because the distribution of the activation energy for charge trapping is wider in the gate-dielectric layer-side of the interface. The presence of a self-assembled monolayer (the ODTS layer) further widened the distribution of the activation energy for charge trapping in gate-dielectric layer-side of the interface and resulted in a more rapid channel current decay. The novel analysis methods presented here enhance our understanding of charge trapping and provide rational guidelines for the development of efficient OFETs with high performance.

4. Experimental Section

Fabrication of the SiO_2-Gated P3HT OFETs: A heavily-doped *n*-Si wafer with a 300-nm-thick thermally grown SiO_2 layer was used as the substrate. The heavily-doped Si layer served as a gate electrode and the SiO_2 served as the gate-dielectric. The measured capacitance of the SiO_2 gate-dielectric was 10.8 ± 0.2 nF cm^{-2} (Figure S1, Supporting Information). The wafer was cleaned in piranha solution for 30 min at 100 °C, then washed with copious amounts of distilled water. The octadecyltrichlorosilane (ODTS, Gelest) self-assembled monolayers were introduced onto the as-cleaned SiO_2 surfaces using the dipping method at 15 °C for 2 h, followed by baking at 170 °C for 15 min to form the ODTS-treated SiO_2 gate-dielectric. This step was skipped when preparing P3HT OFETs without the ODTS layer. Aside from this step, both types of P3HT OFET were prepared via identical processes. Au/Ti (20/3 nm) electrode patterns with a channel width of 1000 μm and a length of 50 μm were thermally deposited onto the gate-dielectric layer through a shadow mask. Finally, 100-nm-thick P3HT (4002-E, Rieke Metals Inc.) was prepared by spin-coating a P3HT solution in chloroform onto the Au patterned substrate.

Fabrication of Vacuum Gap-Gated P3HT OFETs: An additional set of Au contact channels of width 1000 μm and length 50 μm were thermally deposited on top of the as-prepared P3HT film to form source/drain electrodes for the vacuum gap-gated OFET. We separately prepared a vacuum gap gate-dielectric mount equipped with patches for the source/drain and gate contacts and a trough that later served as a vacuum gate-dielectric layer. First, Au/Ti (40/10 nm) gate electrode (the widths of the gate electrodes were 150 μm to fully cover the channel area) patterns were formed on a glass substrate by thermal evaporation through a shadow mask. The SU-8 2005 photoresist (MicroChem) was spin-coated onto the patterned glass substrate, followed by a pre-baking process (at 95 °C for 2 min). The photoresist layer was then selectively exposed to UV light (for 20 s) over the area used for source/drain and the device was submitted to a post-baking process (at 95 °C for 1 min). Another layer of Au/Ti (40/10 nm), which later contacted the source/drain electrodes deposited onto the P3HT layer, was then thermally deposited onto the photoresist film. The device was then submitted to a developing process (2 min in SU-8 developer with sonication) to yield a trough (depth = 5.1 μm, measured using scanning electron microscopy and an alpha-step height measurement system) with a gate electrode on the bottom. A metal-vacuum-metal structure (inset of Figure S1, Supporting Information) was used for measuring the capacitances of the vacuum gap gate-dielectric (0.19 ± 0.04 nF cm^{-2}). Finally, the substrate covered with a P3HT film and including Au top contacts was flipped over and placed on the as-prepared vacuum gate-dielectric mount to form the vacuum gap-gated P3HT OFETs.

Electrical measurements of the OFETs: The electrical performances of the OFETs were characterized using a Keithley 2636A SourceMeter under vacuum (≈10^{-6} Torr). The time resolution of the time-dependent I_D under the gate bias-stress was below 300 ms.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by a grant (no. 2011-0031628) from the Center for Advanced Soft Electronics under the Global Frontier Research Program of the Ministry of Education, Science and Technology, Korea, and the Basic Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2009-0083540).

Received: June 8, 2012
Revised: August 2, 2012
Published online: September 14, 2012

[1] T. Someya, T. Sekitani, *Adv. Mater.* **2010**, *22*, 2228.
[2] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 12321.
[3] G. Gelinck, P. Heremans, K. Nomoto, T. D. Anthopoulos, *Adv. Mater.* **2010**, *22*, 3778.
[4] M. Muccini, *Nat. Mater.* **2006**, *5*, 605.
[5] C. Reese, M. Roberts, M.-M. Ling, Z. Bao, *Mater. Today* **2004**, *7*, 20.

[6] J. A. Lim, F. Liu, S. Ferdous, M. Muthukumar, A. L. Briseno, *Mater. Today* **2010**, *13*, 14.
[7] W. H. Lee, J. H. Cho, K. Cho, *J. Mater. Chem.* **2010**, *20*, 2549.
[8] A. Facchetti, *Mater. Today* **2007**, *10*, 28.
[9] B. J. Jung, N. J. Tremblay, M.-L. Yeh, H. E. Katz, *Chem. Mater.* **2010**, *23*, 568.
[10] I. McCulloch, M. Heeney, M. L. Chabinyc, D. DeLongchamp, R. J. Kline, M. Cölle, W. Duffy, D. Fischer, D. Gundlach, B. Hamadani, R. Hamilton, L. Richter, A. Salleo, M. Shkunov, D. Sparrowe, S. Tierney, W. Zhang, *Adv. Mater.* **2009**, *21*, 1091.
[11] Y. D. Park, J. A. Lim, H. S. Lee, K. Cho, *Mater. Today* **2007**, *10*, 46.
[12] D. Braga, G. Horowitz, *Adv. Mater.* **2009**, *21*, 1473.
[13] J. H. Cho, H. S. Lee, M. Hwang, H. H. Choi, W. K. Kim, J. L. Lee, K. Cho, *Electrochem. Solid-State Lett.* **2007**, *10*, H156.
[14] W. H. Lee, J. A. Lim, D. Kwak, J. H. Cho, H. S. Lee, H. H. Choi, K. Cho, *Adv. Mater.* **2009**, *21*, 4243.
[15] M. E. Gershenson, V. Podzorov, A. F. Morpurgo, *Rev. Mod. Phys.* **2006**, *78*, 973.
[16] M. Pope, C. E. Swenberg, *Electronic Processes in Organic Crystals and Polymers*, Oxford University Press, New York **1999**.
[17] Z. Bao, J. J. Locklin, *Organic Field-Effect Transistors*, CRC Press, Boca Raton, FL, USA **2007**.
[18] M. Uno, K. Nakayama, J. Soeda, Y. Hirose, K. Miwa, T. Uemura, A. Nakao, K. Takimiya, J. Takeya, *Adv. Mater.* **2011**, *23*, 3047.
[19] T. Kaji, T. Takenobu, A. F. Morpurgo, Y. Iwasa, *Adv. Mater.* **2009**, *21*, 3689.
[20] Q. Tang, H. Li, M. He, W. Hu, C. Liu, K. Chen, C. Wang, Y. Liu, D. Zhu, *Adv. Mater.* **2006**, *18*, 65.
[21] S. G. J. Mathijssen, M. Cölle, H. Gomes, E. C. P. Smits, B. de Boer, I. McCulloch, P. A. Bobbert, D. M. de Leeuw, *Adv. Mater.* **2007**, *19*, 2785.
[22] N. T. Nga, M. L. Chabinyc, R. A. Street, A. Salleo, "Bias Stress Effects in Organic Thin Film Transistors", Proceedings 45th Annual IEEE international Reliability Physics Symposium, **2007**. 15–19 April 2007, 2007.
[23] R. A. Street, A. Salleo, M. L. Chabinyc, *Phys. Rev. B* **2003**, *68*, 085316.
[24] S. G. J. Mathijssen, M. Kemerink, A. Sharma, M. Cölle, P. A. Bobbert, R. A. J. Janssen, D. M. de Leeuw, *Adv. Mater.* **2008**, *20*, 975.
[25] M. Tello, M. Chiesa, C. M. Duffy, H. Sirringhaus, *Adv. Funct. Mater.* **2008**, *18*, 3907.
[26] A. Shehu, S. D. Quiroga, P. D'Angelo, C. Albonetti, F. Borgatti, M. Murgia, A. Scorzoni, P. Stoliar, F. Biscarini, *Phys. Rev. Lett.* **2010**, *104*, 246602.
[27] M. Raja, B. Eccleston, *J. Appl. Phys.* **2011**, *110*, 114524.
[28] W. B. Jackson, J. M. Marshall, M. D. Moyer, *Phys. Rev. B* **1989**, *39*, 1164.
[29] T. Miyadera, S. D. Wang, T. Minari, K. Tsukagoshi, Y. Aoyagi, *Appl. Phys. Lett.* **2008**, *93*, 033304.
[30] Y. Chen, V. Podzorov, *Adv. Mater.* **2012**, *24*, 2679.
[31] D. Monroe, *Phys. Rev. Lett.* **1985**, *54*, 146.
[32] V. Podzorov, E. Menard, A. Borissov, V. Kiryukhin, J. A. Rogers, M. E. Gershenson, *Phys. Rev. Lett.* **2004**, *93*, 086602.
[33] Y. Xia, J. H. Cho, J. Lee, P. P. Ruden, C. D. Frisbie, *Adv. Mater.* **2009**, *21*, 2174.
[34] E. Menard, V. Podzorov, S. H. Hur, A. Gaur, M. E. Gershenson, J. A. Rogers, *Adv. Mater.* **2004**, *16*, 2097.
[35] C. D. Dimitrakopoulos, P. R. L. Malenfant, *Adv. Mater.* **2002**, *14*, 99.
[36] H. S. Lee, D. H. Kim, J. H. Cho, M. Hwang, Y. Jang, K. Cho, *J. Am. Chem. Soc.* **2008**, *130*, 10556.
[37] Y. Y. Lin, D. J. Gundlach, S. F. Nelson, T. N. Jackson, *IEEE Trans. Electron Devices* **1997**, *44*, 1325.
[38] J. Takeya, T. Nishikawa, T. Takenobu, S. Kobayashi, Y. Iwasa, T. Mitani, C. Goldmann, C. Krellner, B. Batlogg, *Appl. Phys. Lett.* **2004**, *85*, 5078.
[39] A. Zen, J. Pflaum, S. Hirschmann, W. Zhuang, F. Jaiser, U. Asawapirom, J. P. Rabe, U. Scherf, D. Neher, *Adv. Funct. Mater.* **2004**, *14*, 757.
[40] D. H. Kim, Y. D. Park, Y. Jang, H. Yang, Y. H. Kim, J. I. Han, D. G. Moon, S. Park, T. Chang, C. Chang, M. Joo, C. Y. Ryu, K. Cho, *Adv. Funct. Mater.* **2005**, *15*, 77.
[41] M. S. A. Abdou, F. P. Orfino, Y. Son, S. Holdcroft, *J. Am. Chem. Soc.* **1997**, *119*, 4518.
[42] L. Qiu, W. H. Lee, X. Wang, J. S. Kim, J. A. Lim, D. Kwak, S. Lee, K. Cho, *Adv. Mater.* **2009**, *21*, 1349.
[43] S. G. J. Mathijssen, M.-J. Spijkman, A.-M. Andringa, P. A. van Hal, I. McCulloch, M. Kemerink, R. A. J. Janssen, D. M. de Leeuw, *Adv. Mater.* **2010**, *22*, 5105.
[44] F. R. Libsch, J. Kanicki, *Appl. Phys. Lett.* **1993**, *62*, 1286.
[45] J.-M. Lee, I.-T. Cho, J.-H. Lee, H.-I. Kwon, *Appl. Phys. Lett.* **2008**, *93*, 093504.
[46] T. N. Ng, J. A. Marohn, M. L. Chabinyc, *J. Appl. Phys.* **2006**, *100*, 084505.